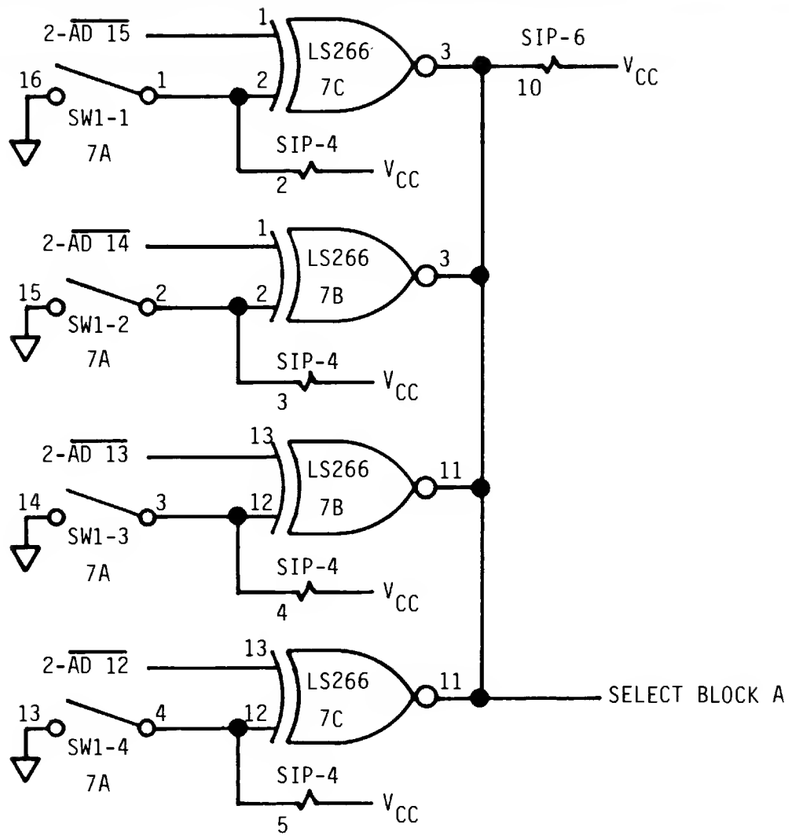

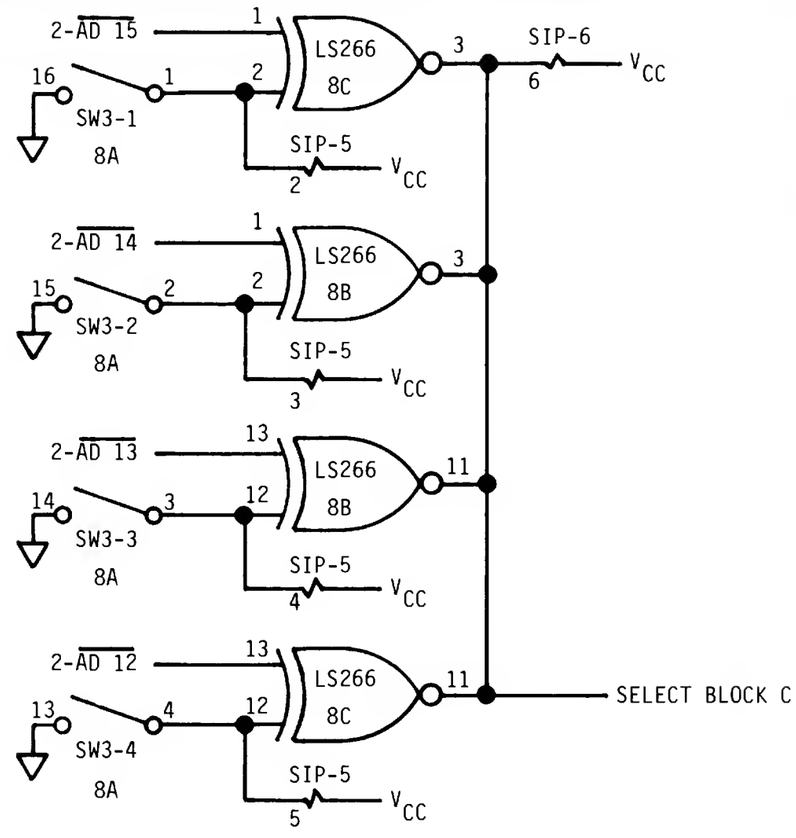

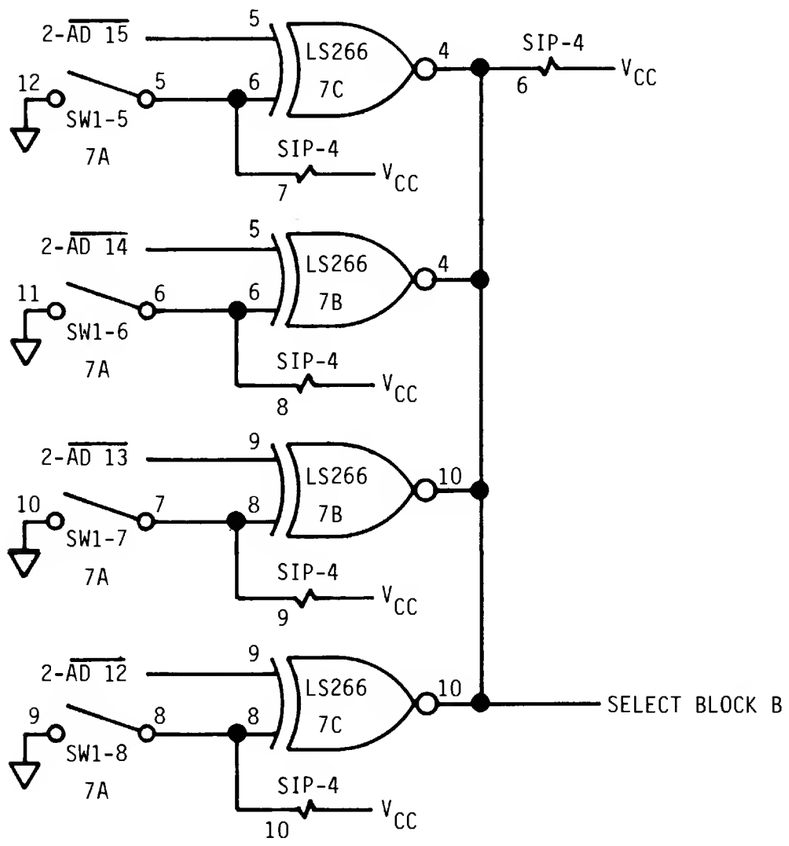

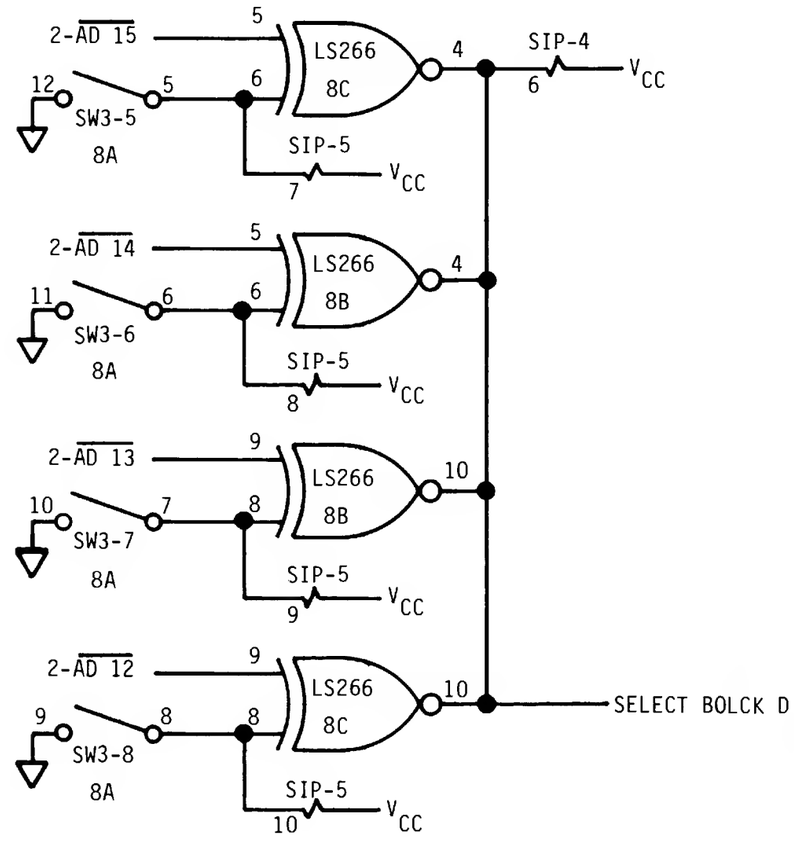

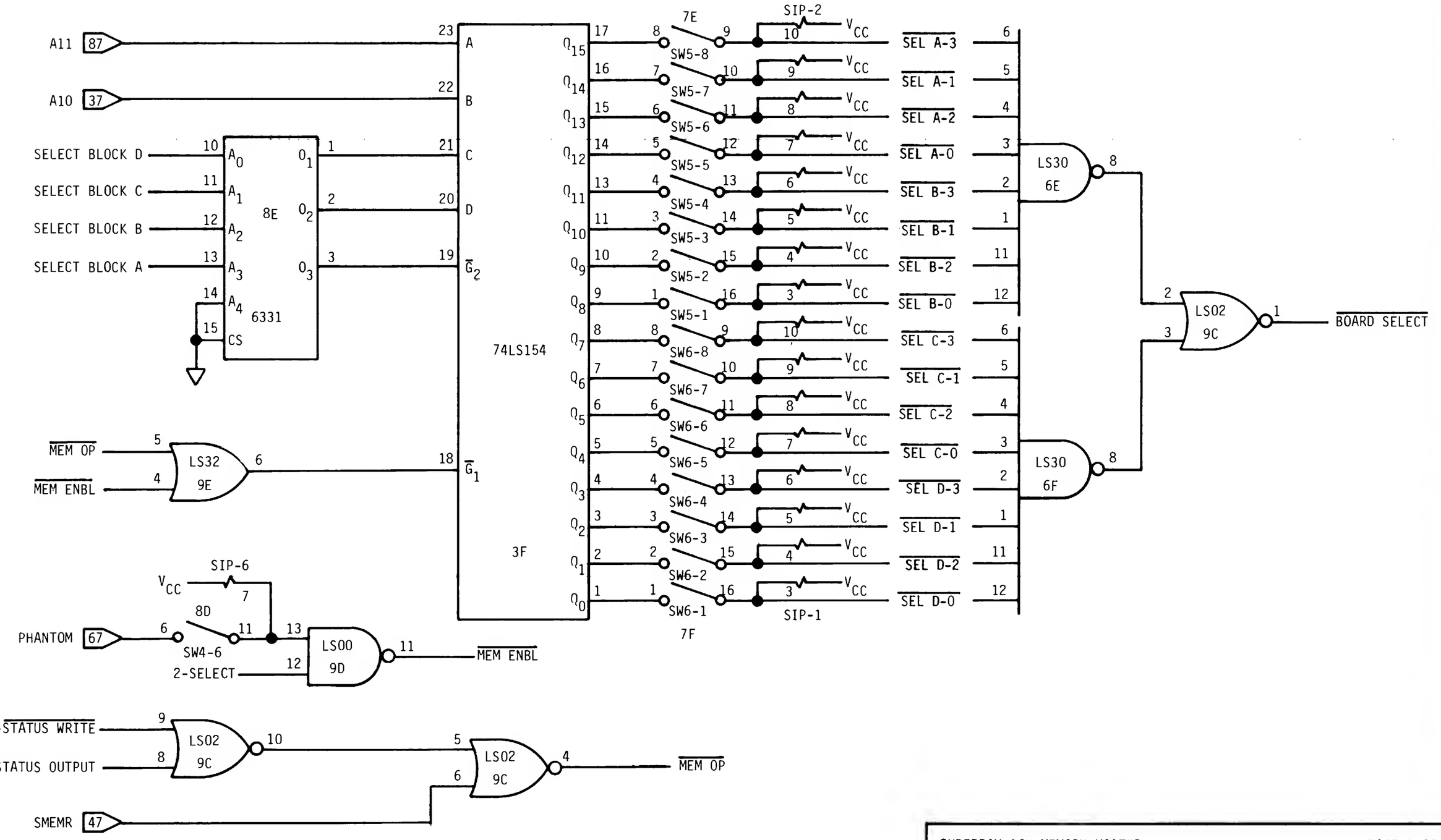

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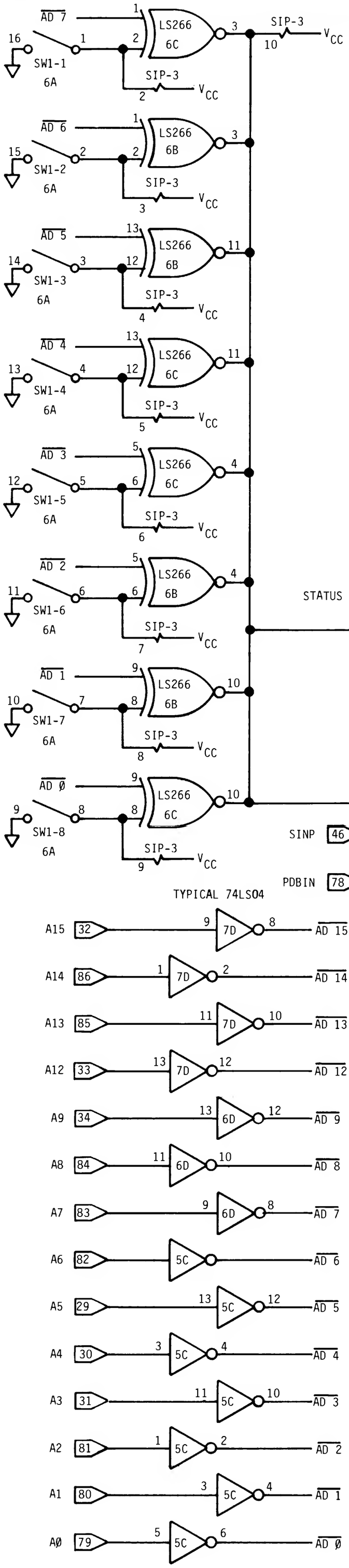
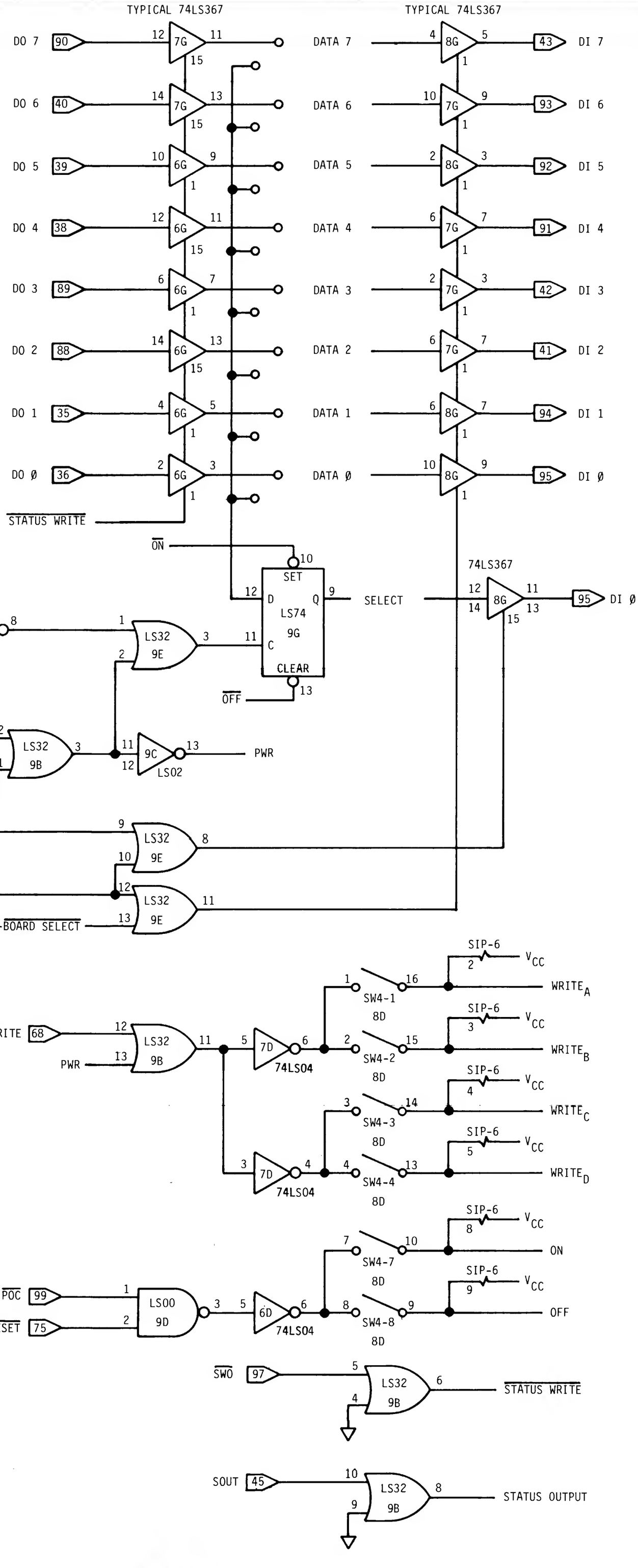
BOARD SELECT LOGIC & BANK SELECT LOGIC — COPYRIGHT 1979 G. MORROW





SUPERRAM 16K MEMORY MASTER

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I/O SELECTION, DATA & ADDRESS BUFFERS

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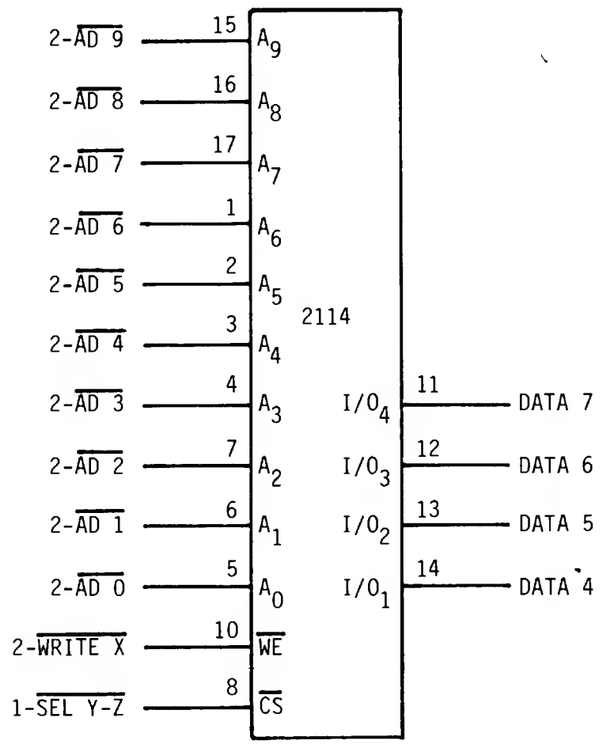
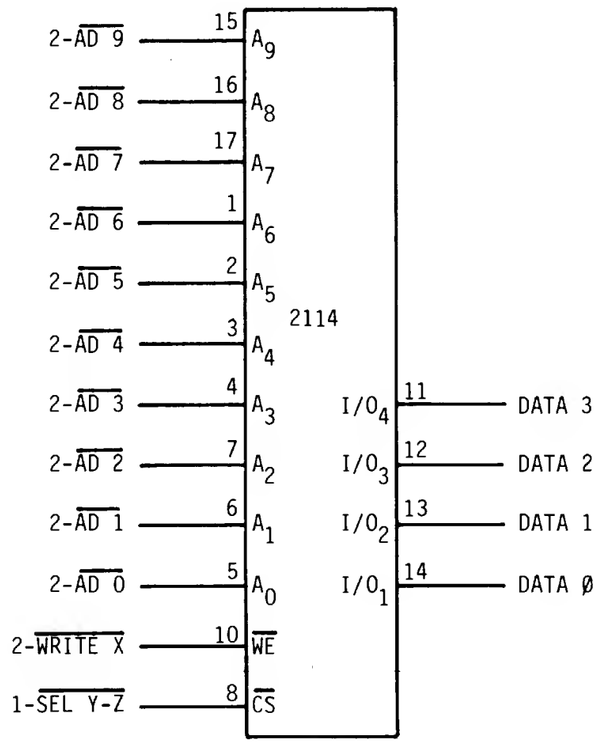
	LOW DATA 1	HIGH DATA 2	LOW DATA 3	HIGH DATA 4	
A	SECTION A BLOCK 0	SECTION A BLOCK 0	SECTION B BLOCK 0	SECTION B BLOCK 0	A
B	SECTION A BLOCK 2	SECTION A BLOCK 2	SECTION B BLOCK 2	SECTION B BLOCK 2	B
C	SECTION A BLOCK 1	SECTION A BLOCK 1	SECTION B BLOCK 1	SECTION B BLOCK 1	C
D	SECTION A BLOCK 3	SECTION A BLOCK 3	SECTION B BLOCK 3	SECTION B BLOCK 3	D
E	SECTION C BLOCK 0	SECTION C BLOCK 0	SECTION D BLOCK 0	SECTION D BLOCK 0	E
F	SECTION C BLOCK 2	SECTION C BLOCK 2	SECTION D BLOCK 2	SECTION D BLOCK 2	F
G	SECTION C BLOCK 1	SECTION C BLOCK 1	SECTION D BLOCK 1	SECTION D BLOCK 1	G
H	SECTION C BLOCK 3	SECTION C BLOCK 3	SECTION D BLOCK 3	SECTION D BLOCK 3	H





SEL A-0, SEL A-1, SEL A-2, SEL A-3 GO WITH WRITE A
SEL B-0, SEL B-1, SEL B-2, SEL B-3 GO WITH WRITE B
SEL C-0, SEL C-1, SEL C-2, SEL B-3 GO WITH WRITE C
SEL D-0, SEL D-1, SEL D-2, SEL D-3 GO WITH WRITE D

MEMORY ARRAY LAYOUT AND TYPICAL BLOCK OF THE ARRAY COPYRIGHT 1979 G. MORROW